PHD:

Advanced Protection of Grid Integrated wind Farms

Due to the simple and non-integrated protection schemes as well as the wind farm construction, different problems arise associated with their protective system. Among these problems, inability to locate the faulty section accurately and unwanted disconnection of wind generation units, rather than disconnecting the faulty unit only, is not acceptable. In this thesis, a detailed dynamic modeling of two complete stages of AL-Zaafarana wind farm was constructed for simulation purposes with the MALAB simulink. Both single fed induction generator (SFIG) and doubly fed induction generator (DFIG) were considered as an example for large wind farms, for protection applications. An experimental wind turbine emulator was implemented in the laboratory in order to realize a better understanding of wind farm behavior. A thorough investigation of the existed protection schemes that are usually utilized with such farms were evaluated considering a wide variety of fault types and locations. To provide these farms with the required proper and integrated protection, two different protection schemes were proposed providing an integrated protection of the overall wind farm circuitry. Current directional-based protection schemes depends on pinpointing the faulty section with sensing the current flow direction before and after the fault inception. The scheme provided an acceptable performance with SFIGs. For DFIGs, the presence of frequency drifting and severe DC decaying remarkably affects its performance. The incremental power flow technique provided a better performance suitable for both SFIG and DFIG farms with a superior efficiency.

2- **Master:**

Analysis and Design of High Performance RTD-CMOS Dynamic Logic Circuits

Abstract

Rapid development in the fields of computers and communications leads to the need for high speed processors. The continuing miniaturization of the conventional CMOS technology faces increasing technological difficulties. Therefore, alternative technologies are needed to provide the required fast processors.

Technologies that contain Resonant Tunneling Diodes (RTDs) can offer a good alternative for high speed applications. RTD has many advantages that make it a promising device. Its operation depends on the tunneling process, which is a very fast process, so it is a suitable device for ultra-high speed applications. Its negative differential resistance (NDR) property makes a remarkable reduction in logic circuits' complexity. RTDs can also be integrated with CMOS technology to improve dynamic CMOS circuits' performance.

Dynamic logic circuits have a higher performance and lower circuit area than their static CMOS counterparts, but they are less noise tolerant. The noise tolerance can be improved using some remedial techniques, such as employing a keeper, on the cost of noticeable performance degradation. RTD-CMOS topology called “smart keeper” was proposed to reduce this performance degradation.

In this work, a brief discussion about RTD modeling is introduced, and different models of I-V and C-V characteristics of RTD are discussed. A simple and accurate SPICE model for RTD is proposed. In addition, a straightforward parameters’ extraction routine is provided. Then, some important applications of RTD like oscillator and inverter are simulated using the proposed model.

A new and effective relationship for sizing of the smart keeper, to achieve a desired I-V characteristic, is derived, verified, and used to design the smart keeper. Then, an overview and classification of the most recent noise-tolerant design techniques of dynamic logic circuits are presented and compared with the smart keeper technique.

A Dual-Rail Domino full adder with the smart keeper is proposed and analyzed using the proposed model in this work